

Logic element based on Electrically Formed Nanowire (EFN) device (Ramot)

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An electrostatically formed nanowire transistor, includes a source, a drain, and multiple gates surrounding a doped silicon region. The gates include a top gate, a bottom gate, and side gates. The gates induce a channel in said doped silicon region. The channel has a width which is decreased by negative biasing of the side gates, and a height and vertical position controlled by the top and bottom gates.

Additional information can be provided upon request.

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